Fine Pitch Cu Pillar Assembly Challenges for Advanced Flip Chip Package

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ABSTRACT
Advanced semiconductor packaging requirements for higher and faster performance in a thinner and smaller form factor continues to grow for mobile, network and consumer devices. While the increase in device input/output (I/O) density is driven by the famous "Moore's Law", the packaging industry is experiencing opposing trends for more complex packaging solutions while the expected cost targets are in a downward trend.

Packaging technology has become more challenging and complicated than ever before, driving advanced silicon (Si) nodes, finer bump pitch as well as finer line width and spacing substrate manufacturing capabilities to satisfy the increasing requirements in the semiconductor industry. As increasing input/output (I/O) counts in a package are needed in mobile devices, packaging solutions are migrating from traditional wire bond packages to flip chip interconnect to meet these requirements. Flip chip chip scale package (fcCSP) is viewed as an attractive solution for complicated and highly integrated systems with multiple functions and heterogeneous mobile applications. Although emerging markets are driving advanced technologies in high performance mobile devices, assembly cost is still the major concern to be addressed.

Due to the rapid growth in emerging markets for mobile applications, advanced Si node technology development with fine flip chip bump pitch for mobile applications is widely viewed as a way to pursue the die size reduction, efficiency enhancement and lower power consumption in the device. Today flip chip bump pitches are reduced to as low as 60µm pitch. Risk for package assembly with traditional mass reflow (MR) is much higher than ever before. Thermal Compresssion Bonding (TCB) can potentially eliminate some of the risks for fine bump pitch. However, lower throughput of TCB which impacts packaging cost is another big concern. This paper will addresses various risk factors for fine bump pitch flip chip assembly, risk mitigation plan, comprehensive assembly and reliability data as well some cost benchmarking.

Key words: flip chip, Cu pillar, fine pitch, mobile, mass reflow, TCB, assembly

INTRODUCTION
As chip technology gets more and more advanced along with the aim toward product miniaturization, the need to reduce the chip package form factor while increasing chip performance has become critical to enabling more advanced chip technology and product miniaturization. Flip chip is the best high density and reliable interconnection technology that is must for fine pitch or ultra-fine pitch (<40um pitch) applications. In today's market the main driver for fine pitch flip chip is mobile and some consumer applications. As demand for increasing input/output (I/O) counts in mobile devices grow, packaging solutions are migrating from traditional wire bond packages to fine pitch flip chip interconnect to meet these requirements. Flip chip chip scale package (fcCSP) is viewed as an attractive solution for complicated and highly integrated systems with multiple functions and heterogeneous mobile applications. Although emerging markets are driving advanced technologies in high performance mobile devices, assembly cost is still another major challenge that always has to be addressed.

Conventional Pb free solder bumps for flip chip packages are on the verge of migrating to fine pitch Cu pillar bumps. As the bump pitch size shrinks, solder bumps have many limitations in the fine pitch process. Bump printing, plating or bump drops along with bump pad sizes are the major constrains. Due to the cylindrical shape and non-collapsing nature of Cu pillar bumps, they can be easily mounted on the fine trace of the laminate. Typically a tiny solder cap is used in the Cu pillar bump. Too small of a solder cap can potentially cause solder smearing or extrusion during the assembly process which could lead to bridging or shorting for fine pitch applications. An alternative to Cu pillar bump is metal to metal bonding such as Cu-Cu or Au bumps which can be used for ultra-fine pitch applications. However, metal-metal requires a very precise process and capital investment. Metal-metal is exceptionally prone to oxidization and is very difficult to make strong bond. Figure 1 shows a representative picture of miniaturization of traditional, Pb free, and Cu pillar bumps for fine pitch flip chip applications.

In the conventional flip chip bonding process, both the copper and solder bumps are self-aligned in between the die and substrate in a standard reflow or mass reflow (MR) manufacturing process to achieve high production yields.

However, there is a high risk for cracking or delamination of the very fragile extremely low-k (ELK) layer or the advanced Si node and bump cracking in the manufacturing process, other failures are bump and die cracking, and bump bridging in the underfill fill steps. One of the root causes of the failures is that the traditional reflow process introduces very high thermal stresses during the chip attach process. To address these kinds of issues and to simplify the manufacturing processes for the next generation fine pitch flip chip, thermal compression bonding (TCB) or thermal compression with non-conductive paste (TCNCP) was introduced into the assembly process. Each process has some merits and demerits. For the conventional flip chip manufacturing process, more assembly process steps are involved such as die preparation (DP), chip attach, reflow, flux cleaning or deflux, baking, underfill and underfill curing, and the molding if needed.

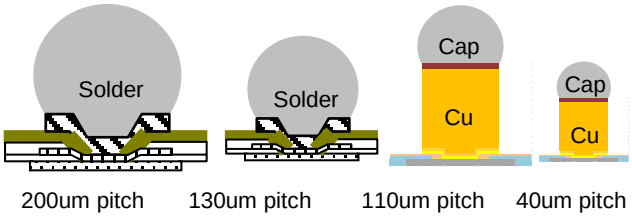

Figure 1: Flip chip bump miniaturization typical data

With the application of TCNCP, two to three processing steps can be reduced as shown in Figure 2. Before the thermal compression bonding with pre-applied NCP, the TCNCP goes through the die preparation (DP) which is the same as a conventional flip chip manufacturing process. The DP involves wafer back grinding and laser grooving which separates each die from the wafer. After the DP, the substrate in the TCNCP process is then baked to remove the moisture and prevent voiding risks. Following the substrate baking, the substrate is cleaned with a plasma cleaning process to remove surface impurities and achieve a better surface adhesion for compression bonding and better flow of NCP materials. Figure 3 also shows that with the TCNCP process, the reflow and deflux steps are removed which ultimately lowers assembly cost.

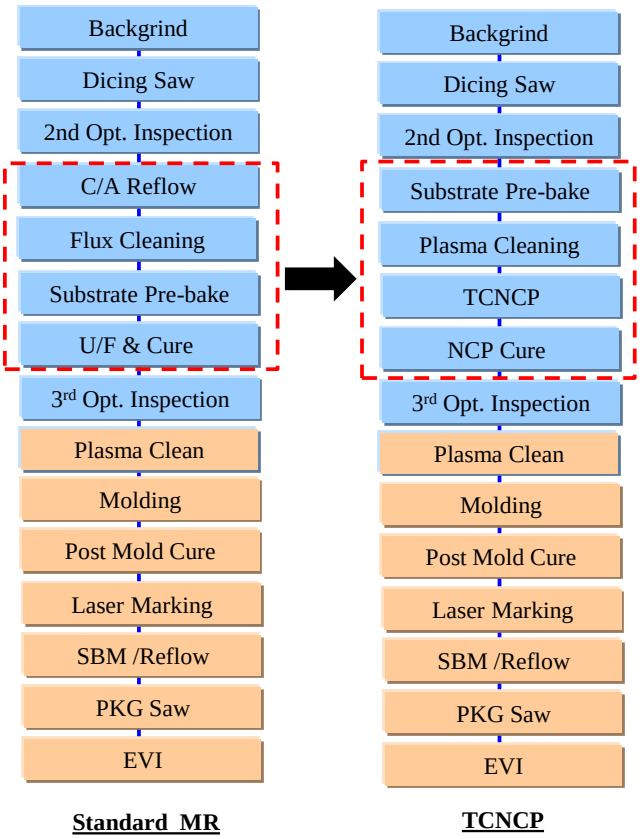

Figure 2: Conventional reflow (MR) vs TCNCP assembly process

NCP is a pre-dispensed paste type material. In order to achieve good interconnection, the right bonding force and temperature profile the key for TCNCP. The right NCP material selection is important to eliminate voiding during the assembly process.

Recently for fine pitch applications, the industry is moving towards thermal compression without NCP material. The process is often referred as thermal compression with capillary underfill (TCCUF). Here, a typical post dispense copper underfill (CUF) is used after thermal compression bonding which replaces NCP material and hence achieves a void free underfill for fine pitch Cu pillar applications.

Another new technology very recently introduced in the market for fine pitch bump interconnection is called laser assisted bonding (LAB). In this technology an infra-red (IR) laser is used to heat up the entire die only and make a good interconnection joint between the die to substrate. The time required to attach the die with the substrate is significantly lower than MR or TCNCP. As a result, LAB provides much better throughput than TCNCP. In terms of the assembly process, there is no difference between MR and LAB except the MR reflow process is interchanged with LAB (Figure 3). Both CUF and molded underfill (MUF) can be used in the LAB process. LAB process substrates don't need to be heated, therefore, it only takes only a few seconds to heat up the die. As a result, there is very low thermal stress involved

in the process. Figure 4 shows a typical cross-section picture of bumps for various interconnection technologies. No significant warpage, bump tearing, non-wet, or bump alignment was observed in the LAB process. In the TCNCP process, there is a big risk of solder extrusion, bridging or bump tearing due to the excessive bonding force of thermal compression in the process. Very little force is applied in the LAB process and hence there is no big concern of solder extrusion which clearly observed in Figure 4 below.

Chip Package Interaction (CPI) with Fine Pitch

In high-performance semiconductors, the back-end-of-line (BEOL) interconnect pitch has been shrinking due to Moore's law. Performance and advancement of the IC chips can never be achieved without addressing various reliability risks of the IC and packages. The coefficient of thermal expansion (CTE) between die and package materials and mismatch induces thermo-mechanical stresses at the interfaces during thermal excursions, which can compromise the chip's structural integrity. The influence of the package-induced stress on the chip is called chip-package interaction (CPI), and it plays a very critical role in overall product design and reliability. In order to meet advanced electrical requirement of the IC device, the industry now uses ULK or ELK dielectrics along with Cu interconnect. The mechanical strength of dielectric material becomes very weak due to fragile nature of the ULK or ELK, therefore, thermo-mechanical reliability has been a challenge. Typical failure modes observed in the CPI studies are ultralow-k or extreme low-k fracture or crack, delamination, under bump metallurgy (UBM) delamination, passivation layer cracking, bump tear, etc.

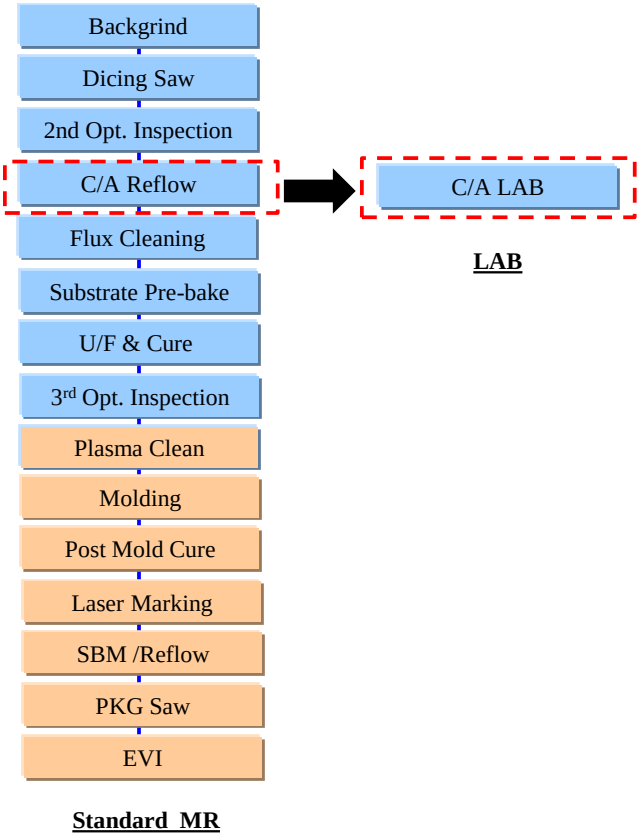

Figure 3: LAB process replaces conventional MR

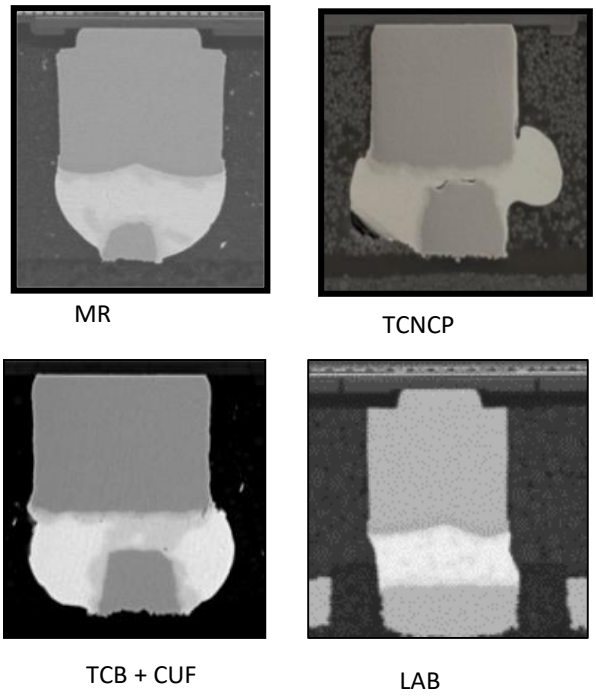

Figure 4: Typical fine pitch Cu pillar bump cross-section data with various attach technologies

Fine Pitch Cu Pillar CPI

In this study a 15x15mm flip chip fine BGA fcFBGA) with advanced ELK backend process daisy-chain die is used as

the test vehicle to collect CPI data using mass reflow process. A die size of ~135mm^2 with 200um, and 65um die thickness was used in the design of experiment (DOE). Cu pillar was designed with 90um and 60um bump pitch and a 58um Cu pillar height with escape trace between the bump. Two different die thicknesses (200um and 65um) were considered in the DOE to compare the die thickness effect in 10nm CPI work. The package was mounted on a very thin two layer (2L) substrate with a total thickness of 0.15mm. . A typical package schematic is shown in Figure 5.

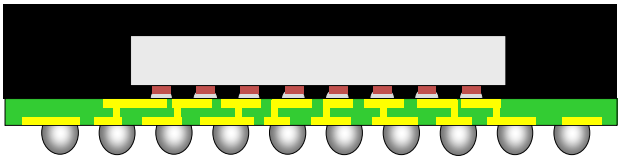

Figure 5: Package schematic for CPI work

Standard quick temperature cycle (QTC) @ -40 to 60C temperature range and 30C ramp up/down with 5 minutes dwell time was conducted to make sure the Si robustness was captured in the CPI work. MR with POR (process of record) reflow profile and slow cooling reflow profile or modified reflow profile (MRP) are studied in the DOE. Results found that MRP helped a lot to fix the ELK crack issue as shown in Table 1. It was found that all samples with MR failed QTC and didn't pass QTC 60x. This result shows that the ELK performance is significantly impacted with the Reflow profile parameters.

Table 1: Fine pitch Cu pillar QTC DOE using mass reflow

		QTC (-40 to 60C) Results						
Leg	**Attach Technology**	**0x**	**10x**	**20x**	**30x**	**40x**	**50x**	**60X**
1	MR	pass	pass	pass	pass	fail		
2	MRP	pass	pass	pass	pass	pass	pass	pass

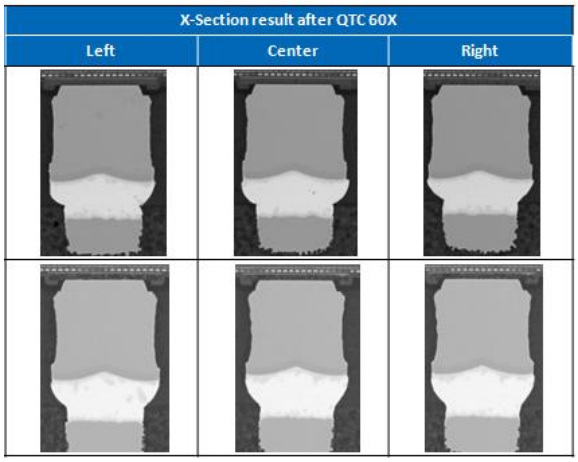

Figure 6: Bump Cross-section after QTC 60X readpoint with MRP

The effect of die thickness was also captured in the DOE for MR process only. The investigation found that a thicker die is more prone to ELK crack than a thinner die due to stress. Thin die is much more complaint than a thicker die and hence, ELK stress is lower. Table 2 shows the data of die thickness effect. In fact, the ELK failure with thicker die was observed in the assembly process prior to QTC test. A failure analysis has been conducted to capture the failure mode. Figure 7 shows typical ELK failure of thicker die right after the assembly process. No ELK crack was observed in thin die as shown in Figure 8 below.

Table 2: Die thickness effect

					QTC (-40 to 60C)	
Attach Technology	**Substrate layer**	**Substrate thk (um)**	**Die thk (um)**	**Pitch (um)**	**0X**	**20X**
MR	2L	150	65	60	pass	fail
MR	2L	150	200	60	fail	

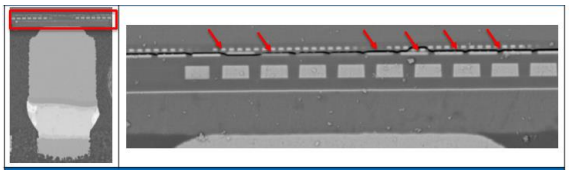

Figure 7: ELK crack with thicker die (200um, 60um pitch w/ MR) right after assembly

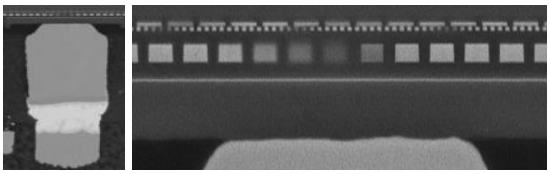

Figure 8: No ELK crack with thin die (65um, 60um pitch w/ MR) right after assembly

As the flip chip bump pitch is reduced to 60µm, the risk of a solder bridge during the chip attach process will be more challenging, expecially when there is escape trace between the bumps. With the TCNCP and LAB process, the risk level potentitally can be minimized. A die shear test was conducted after the chip attach process to ensure no solder brdiging or non-wet in the bumps. Package level warpage as well as JEDEC standard component level comprehensive reliability tests were conducted with the MRP.. Figure 9 illustrates the warpage distribution for various temperature read points in the package with 60µm bump pitch and MRP process. In this figure, the corresponding warpage distribution is well within the specification. The long term reliability tests such as MSL3 pre-condition with uHAST 96 hours, TCB 1000 cycles and HTST 1000 hours were also performed to demonstrate package reliabilty, as shown in Figure 9. No anomalies were observed in various test condtions as shown in Figure 10.

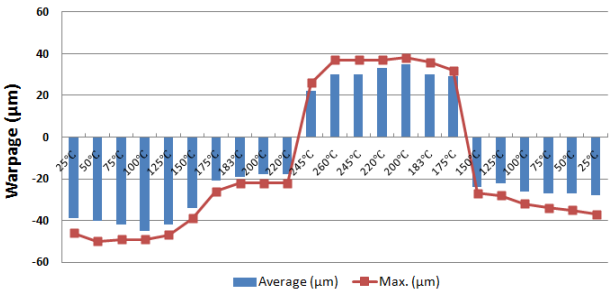

Figure 9: Package warpage with temperature for 60um bump pitch, MRP process

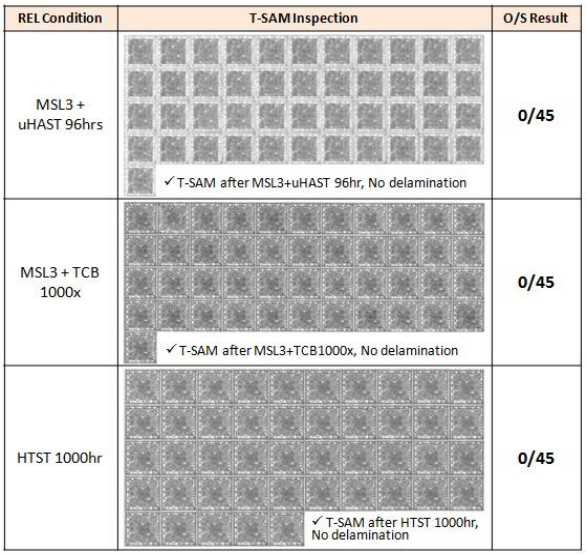

Figure 10: Fine pitch fcFBGA long term reliability data with MRP process

To prove LAB technology for fine pitch Cu pillar applications, a few other test vehicles (TV) were built to collect more CPI data, process margin and comprehensive reliability. One of the examples was a fcFBGA package with 13X13mm body size, 8X9mm die size with 16FF silicon and 85um Cu pillar bump pitch with one trace between the bumps. Similar to the previous 60um bump pitch program QTC, CSAM, warpage and JEDEC standard full package reliability were also performed as shown in Table 3 and bump cross-section pictures are in Figure 11 below. There was no anomaly in the bump structure and the joints are perfectly aligned.

Table 3: Fine pitch fcFBGA long term reliability data with LAB process

PKG	Si Node	Bump Pitch (um)	Reliability (Electrical O/S test)						
			MRT L3	TC'B'		uHAST		HTST	
				500X	1000X	96h	192h	500h	1000h
fcFBGA (13X13mm)	16N	85	0/80 (pass)	0/40 (pass)	0/40 (pass)	0/40 (pass)	0/40 (pass)	0/40 (pass)	0/40 (pass)

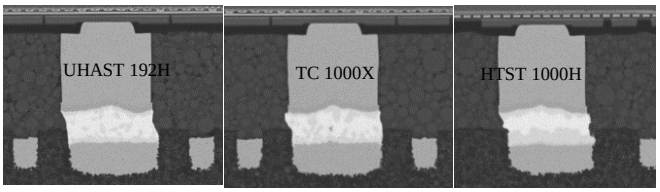

Figure 11: Fine pitch Cu pillar bump cross-section data after standard reliability tests

Fine Pitch Cu Pillar in fcBGA

Fine pitch Cu pillar bump has experienced growing adoption in high performance and low-cost area array flip chip BGA (fcBGA) packages as well. In area array bumps, assembly challenges are much more prevalent than typical perimeter array fcFBGA packages. Similar to perimeter array fcFBGA bumps, TCNCP is one of the alternative solutions for fine pitch bumps in fcBGA. However, the cost, bump misalignment and ELK crack are still major concerns here. In this study LAB technology was also investigated for several area array fine pitch bump fcBGA packages. Very similar results were found in fcBGA packages. For a 17X17mm fcBGA with a heat spreader (fcBGA-H) and 4 MCM dies that were each 7X5mm in size and 60um UBM, a 180um Cu pillar bump was used in the TV. A relatively thicker die (350um) was used for the TV. Both MR and LAB processes were used in the study. The temperature profile for LAB at various locations on the packages were measured and plotted as shown in Figure 12. The maximum temperature location was in the die while the minimum was in the substrate. There was no significant temperature gradient observed in the substrate. Total reflow time was a little over 1 sec.

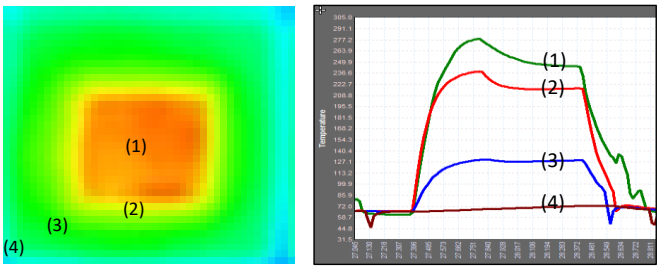

Figure 12: Temperature gradient in the die for LAB process

Side by side comparison was data collected for LAB using the same fcBGA-H TV. QTC test was conducted on the bare bump package. As expected, the MR leg failed as low as 20X QTC read point whereas LAB survived up to 60X read points. Table 4 shows the QTC data between the legs. Package final test was also completed for LAB process and achieved 100% assembly yield even for a small sample size.

Table 4: fcBGA-H CPI QTC data w/ LAB process

Process	Die thk	QTC (-40 to 60C)						
		0X	10X	20X	30X	40X	50X	60X
MR	350um	pass	pass	fail	-	-	-	-
LAB		pass	pass	pass	pass	pass	pass	pass

A small number of units from each leg (MR and LAB) were selected for destructive failure analysis (FA) and intermetallic morphology analysis. The IMC growth mechanism in this study is illustrated in Figure 13. At reflow stage, Ni-Sn IMC was formed at the interface between the Ni layer and solder, and Cu-Sn IMCs were formed at the bonding interface between Cu pad and solder. In comparing the two pictures, it is somewhat clear that less IMC formed with LAB process as compared to MR due to longer thermal exposure of MR during the attach process. More investigation will be required to verify it.

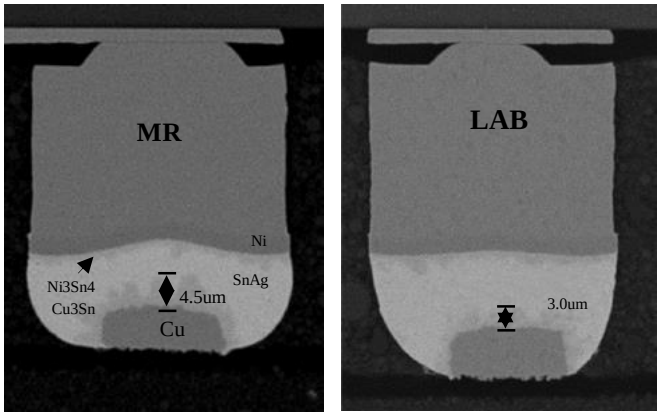

Figure 13: IMCs growth behaviors between the two processes

CONCLUSION

With the phenomenal expansion of various fine pitch Cu pillar attach technology offerings and manufacturing footprints, assembly suppliers are positioning themselves to support the strategic need for very cost effective, high performance packages for various fine pitch applications. With the evolution of different new flip chip attach technologies, it is expected that significant cost can be associated with the new technology to overcome assembly related yields. Standard MR to latest LAB attach technologies were described in the paper.

Several case studies with fine pitch Cu pillar bumps were considered in this study. The QTC test with temperature range of -40˚C to 60˚C along with JEDEC standard reliability tests were perfomeed to confirm if there was any white bump phenomenon in the CPI work or any other long term reliability related failures. Invariably, all the cases found that MR has minimal limitations for very fine pitch Cu pillar assembly process. LAB is a new technology that can potentially be used as an alternative to MR for very fine pitch applications. However, the industry is will continue to extend the MR process window to make a robust and cost effective solution for fine pitch flip chip. From the literature, a conclusion can be reached that MR has the highest throughput as compared to LAB or TCNCP. Typically, TCNCP is about one quarter to one third of MR and LAB is about half to three fourth for MR. More investigation and further study is needed to support the above statement.

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